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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/608,869	06/30/2000	Stephen S. Chang	042390.P8815	2389

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EXAMINER	
BANANKHAH, MAJID A	

ART UNIT	PAPER NUMBER
2127	8

DATE MAILED: 04/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/608,869	CHANG, STEPHEN S.	
	Examiner	Art Unit	
	Majid A Banankhah	2127	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-30 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-30 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. This final office action in response to paper number 7, Amendment A that was filed dated January 20, 2004. Claims 1-30 are presented for examination. Applicants' argument has been fully considered but they are not deemed to be persuasive.

2. The text of those sections of Title 35, U.S. code not included in this office action can be found in a prior Office action.

3. The rejection of claims 1-30 stated in the previous Non-Final Office Action dated January 20, 2004 is hereby incorporated.

4. Response to the Remarks;

(i) Applicant in his remarks argue:

"*Brown does not disclose, either expressly or inherently, (1) a block allocation circuit to allocate blocks of cache memory used by at least one of the task, and (2) a task coordinator to coordinate the tasks in response to a task cycle issued by the processor*".

In response, applicant's attention is directed to the teaching of Brown in col. 10, line 48-57 where he teaches of buffer allocation in the memory at the time of execution, regarding block allocation table. He also teaches of task coordinator in col. 6, lines 62-65, where he teaches of interrupt routine which passes control data to the execute routine. Interrupt routine is a inseparable part of any operating system which coordinate the task and works bases on the processors cycle.

(ii) Later Applicant argue:

"*Brown merely discloses an executive routine (EXEC) for memory management, not a block allocation circuit. The EXEC routine is the operating system that interfaces to and manages the individual signal-processing block of code (Brown, col. 11, lines 59-61). It is generally programmed by the MCU (Brown, col. 11, line (57)*".

In response, to the argument related to allocation circuit as opposed to allocation program, it is submitted that "product by process claims are not limited to the manipulation of the recited steps, only to the structure limited by the steps". Therefore,

the patentability of a product does not depend on its method of production. If the product in the product-by process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process.

(iii) Later applicant argues:

"Since it is merely a program, it is not a circuit coupled to the bus interface and a cache memory. Furthermore, the EXEC routines merely allocate the data buffers and data streams. It does not allocate blocks of cache memory. The Examiner further states that Brown disclose a task coordinator to coordinate the tasks in response to a task cycle issued to the processor. Applicant respectfully disagrees. Brown merely discloses a timer to provide a computer-triggered output to other blocks by a direct signal or a write/read (W/R) cycle through the DFP (Brown, col. 11, lines 1-3). A W/R cycle is not a task cycle issued by a processor. As described in the Specification, a task cycle transfers the information and data of a task on the system bus (See Specification, page 9, line 13). It may be either of loading a task or of executing a task (See Specification, page 14, lines 2-3; lines 8-25)".

In response, it is submitted that, Brown teaches of the limitation in col. 9, lines 65-68 to col. 10, lines 1-8 (*The interrupt routine and executive routines will store the information on each task. Examples of information sent to DSP's 300 executive routine are: task ID, data stream number, and memory management data).*

(iv) Later Applicat argues:

"Claims should be interpreted consistently with the specification, which provides content for the proper construction of the claims because it explains the nature of the patentee's invention. See Renishaw, 158 F.3d 1250. :During patent examination, the pending claims must be "given the broadest reasonable interpretation consistent with the specification". See MPEP 211 1. The terms "task", "task entries", "task table", "block allocation circuit," "task coordinator" and "task cycle" should be interpreted consistently with the specification such as provided on page 3 (lines 15-20, lines 23-26). page 7 (lines 12-25), page 8 (lines 1-7), page 9 (lines 3-13), and page 14 (lines 2-3, lines 8--23). To anticipate a claim, the reference must teach every element of a the claim. "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.

In response, it is submitted that the Examiner's claim construction is consistent with the specification. In that regard, Applicants attention is directed to the teaching "task", "Task table", "block allocation table", "task coordinator", and "Task cycle", in col. 3, lines 3-11 (for **task**), Fig. 24 Task Status (for **task table**, see status of the tasks), col. 6, lines 62-65 (**for task coordinator**), and in col. 9, lines 65-68 to col. 10, lines 1-8 (for task cycle, according to the specification).

(v) Applicant later argues:

"*Brown, Tuma and Nagata, taken alone or in any combination, does not disclose, suggest, or render obvious (1) a block allocation circuit to allocate blocks of cache memory used by at least one of the task, (2) a task coordinator to coordinate the tasks in response to a task cycle issued by the processor, (3) a search logic circuit to locate a free block, and (4) a block information generator to generate block information.*"

In response, it is submitted that Brown teaches "block allocation table", "task coordinator", and "task cycle" as stated above. With regard to the search logic, Applicant's attention is directed to the teaching of Nagata in col. 4, lines 10-45, and Fig. 23, and 24, where he teaches update buffer status and free block retrieve table. Regarding the block information generator table, see Brown, Fig, 23, and 24, and Fig. 11 (See the chart, buffer begins and buffer ends, and in Fig. 11, program memory and block information).

(vi) on page 10, Applicant argues:

"*Brown does not disclose or suggest a block allocation circuit and a task coordinator as discussed above. Tuma merely discloses an address, generator for a SCSI peripheral device. The stating address is used for reading or writing a logical block (Tuma, col. 4, lines 17-21). This is not the same as the task start address corresponding to a task: Nagata merely discloses flags to indicate unused blocks among the bit map font blocks (Nagata, col. 4, lines 42-45). The font blocks are part of the SRAM. They do not correspond to data blocks in use in the cache memory as recited in claim 4, 14, and 24. Furthermore, none of Brown, Tuma, and Nagata discloses a search logic circuit to locate a free block arid a block information generator to generate block information including a block size, a block starting address, and a block ending address.*"

In response, it is submitted that finding the start and end address of a block of memory for read and write is not different from finding the start and ending address of a task. How, it is possible to be able to fine the start and end address of a block of memory but not be able to find the start and end address of the memory of a task. Applicant should argue why the finding of the beginning and ending of a block of memory for read and write is different from finding the beginning and ending of the memory associated with a task.

(vi) later Applicant argues:

"*There is no motivation to combine Brown, Tuma and Nagata because neither of them addresses the problem of task-based multiprocessor system. There is no teaching or suggestion that a block allocation circuit or a task coordinator is present. Brown, read as a whole, does not suggest the desirability of allocating cache memory or coordinating tasks in response to a task cycle". In the present invention, the cited references do not*

expressly or implicitly suggest (1) a block allocation circuit to allocate blocks of cache memory used by at least one of the task, (2) a task coordinator to coordinate the tasks in response to a task cycle issued by the processor, (3) a task status, identifier, start address, block size, and task cache address; and (4) a search logic circuit and a block information generator. In addition, the Examiner failed to present a convincing line of reasoning as to why a combination of Brown, Tuma and Nagata is an obvious application of a task-based multiprocessor system."

In response, regarding the "block allocation circuit" and "task coordinator", "task status identifier [task table], Applicant's attention is directed to section (i) and (iv) above.

5. The prior art made of record and not relied upon is considered pertinent to

applicant's disclosure.

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 C.F.R. § 1.136(a).

A SHORTENED STATUTORY PERIOD FOR RESPONSE TO THIS FINAL ACTION IS SET TO EXPIRE THREE MONTHS FROM THE DATE OF THIS ACTION. IN THE EVENT A FIRST RESPONSE IS FILED WITHIN TWO MONTHS OF THE MAILING DATE OF THIS FINAL ACTION AND THE ADVISORY ACTION IS NOT MAILED UNTIL AFTER THE END OF THE THREE-MONTH SHORTENED STATUTORY PERIOD, THEN THE SHORTENED STATUTORY PERIOD WILL EXPIRE ON THE DATE THE ADVISORY ACTION IS MAILED, AND ANY EXTENSION FEE PURSUANT TO 37 C.F.R. § 1.136(a) WILL BE CALCULATED FROM THE MAILING DATE OF THE The application has been amended as follows:
ADVISORY ACTION. IN NO EVENT WILL THE STATUTORY PERIOD FOR RESPONSE EXPIRE LATER THAN SIX MONTHS FROM THE DATE OF THIS FINAL

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Maid A. Banankhah** whose voice telephone number is **(703) 308-6903**. A voice mail service is also available at this number.

All response sent to U.S. Mail should be mailed to:
Commissioner of Patent and Trademarks
Washington, D.C. 20231

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is **(703) 305-9600**.

Majid A. Banankhah

4/19/04

MAJID BANANKHAH
PRIMARY EXAMINER